CLAIMS

WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit comprising:

a bias circuit that has a first current source for generating a first current and a load circuit connected in series with the first current source, and that generates a first voltage at a first node that is a connecting node between the first current source and the load circuit;

a second current source that generates a power supply current in accordance with the first voltage;

an internal circuit that has a plurality of first transistors and is connected to said second current source in order to operate the first transistors; and

a correcting circuit that includes a correcting transistor receiving a constant voltage at a gate, and that generates, in accordance with the constant voltage, a correcting current at a second node electrically connected to a drain of the correcting transistor, the second node being electrically connected to the first node.

2. The semiconductor integrated circuit according to claim 1, wherein:

said bias circuit has a reference voltage generator that has

a threshold voltage compensating function for a variation of a threshold voltage of each of the first transistors formed in said internal circuit and

a temperature compensating function for a temperature variation,

said reference voltage generator generating a constant reference voltage independently of the temperature variation and the variation of the threshold voltage; and

said bias circuit generates the first voltage in accordance with the reference voltage.

3. The semiconductor integrated circuit according to claim 2, wherein

the reference voltage generator is a band-gap reference.

4. The semiconductor integrated circuit according to claim 1, wherein the correcting transistor is an nMOS transistor.

5. The semiconductor integrated circuit according to claim 1, wherein the correcting transistor is a pMOS transistor.

6. The semiconductor integrated circuit according to claim 1, wherein:

said first current source and said second current source have a second transistor and a third transistor respectively whose gates are connected to the first node; and

the second transistor and the third transistor constitute a first current mirror circuit.

7. The semiconductor integrated circuit according to claim 1, wherein a drain of the correcting transistor is directly connected to the second node.

8. The semiconductor integrated circuit according to claim 1, wherein:

a drain of the correcting transistor is connected to each gate of a pair of fourth transistors constituting a second current mirror circuit; and

a drain of one of the fourth transistors that is not connected to the correcting transistor is connected to the second node.

9. A semiconductor integrated circuit comprising:

a bias circuit that has a first current source for generating a first current and a load circuit connected in series with the first current source, and that generates a first voltage at a first node that is a connecting node between the first current source and the load circuit;

a second current source that generates a power supply current in accordance with the first voltage;

an internal circuit that has a plurality of first transistors and is connected to said second current source in order to operate the first transistors; and

a correcting circuit that includes a correcting transistor receiving a constant voltage at a gate, and that generates, in accordance with the constant voltage, a correcting current at

a second node electrically connected to a drain of the correcting transistor, the second node being connected to a connecting node between said second current source and said internal circuit.

10. The semiconductor integrated circuit according to claim 9, wherein:

said bias circuit has a reference voltage generator that has

a threshold voltage compensating function for a variation of a threshold voltage of each of the first transistors formed in said internal circuit and

a temperature compensating function for a temperature variation,

said reference voltage generator generating a constant reference voltage independently of the temperature variation and the variation of the threshold voltage; and

said bias circuit generates the first voltage in accordance with the reference voltage.

11. The semiconductor integrated circuit according to claim 10, wherein

the reference voltage generator is a band-gap reference.

12. The semiconductor integrated circuit according to claim 9, wherein

the correcting transistor is an nMOS transistor.

13. The semiconductor integrated circuit according to claim 9, wherein

the correcting transistor is a pMOS transistor.

14. The semiconductor integrated circuit according to claim 9, wherein:

said first current source and said second current source have a second transistor and a third transistor respectively whose gates are connected to the first node; and

the second transistor and the third transistor constitute a first current mirror circuit.

15. The semiconductor integrated circuit according to claim 9, wherein

a drain of the correcting transistor is directly connected to the second node.

16. The semiconductor integrated circuit according to claim 9, wherein:

a drain of the correcting transistor is connected to each gate of a pair of fourth

transistors constituting a second current mirror circuit; and

a drain of one of the fourth transistors that is not connected to the correcting transistor is connected to the second node.

17. A semiconductor integrated circuit comprising:

a bias circuit that has a first current source for generating a first current and a load circuit connected in series with the first current source, and that generates a first voltage at a first node that is a connecting node between the first current source and the load circuit;

a second current source that generates a power supply current in accordance with the first voltage;

an internal circuit that has a plurality of first transistors and is connected to said second current source in order to operate the first transistors;

a first correcting circuit that includes a first correcting transistor receiving a first constant voltage at a gate, and that generates, in accordance with the first constant voltage, a first correcting current at a second node electrically connected to a drain of the first correcting transistor; and

a second correcting circuit that includes a second correcting transistor receiving a second constant voltage at a gate and having a reverse polarity to a polarity of the first correcting transistor, and that generates, in accordance with the second constant voltage, a second correcting current at the second node electrically connected to a drain of the second correcting transistor, wherein

the second node is electrically connected to the first node.

18. The semiconductor integrated circuit according to claim 17, wherein:

said bias circuit has a reference voltage generator that has

a threshold voltage compensating function for a variation of a threshold voltage of each of the first transistors formed in said internal circuit and

a temperature compensating function for a temperature variation,

said reference voltage generator generating a constant reference voltage independently of the temperature variation and the variation of the threshold voltage; and

said bias circuit generates the first voltage in accordance with the reference voltage.

19. The semiconductor integrated circuit according to claim 18, wherein

the first constant voltage generator is a band-gap reference.

20. The semiconductor integrated circuit according to claim 17, wherein

one of the first correcting transistor and the second correcting transistor is an nMOS transistor, and the other is a pMOS transistor.

21. The semiconductor integrated circuit according to claim 17, wherein:

said first current source and said second current source include a second transistor and a third transistor respectively whose gates are connected to the first node; and

the second transistor and the third transistor constitute a first current mirror circuit.

22. The semiconductor integrated circuit according to claim 17, wherein:

a drain of the first correcting transistor is directly connected to the second node;

a drain of the second correcting transistor is connected to each gate of a pair of fourth transistors constituting a second current mirror circuit; and

a drain of one of the fourth transistors not connected to the correcting transistor is connected to the second node.

23. A semiconductor integrated circuit comprising:

a bias circuit that has a first current source for generating a first current and a load circuit connected in series with the first current source, and that generates a first voltage at a first node that is a connecting node between the first current source and the load circuit;

a second current source that generates a power supply current in accordance with the first voltage;

an internal circuit that has a plurality of first transistors and is connected to said second current source in order to operate the first transistors;

a first correcting circuit that includes a first correcting transistor receiving a first constant voltage at a gate, and that generates, in accordance with the first constant voltage, a first correcting current at a second node electrically connected to a drain of the first correcting transistor; and

a second correcting circuit that includes a second correcting transistor receiving a second constant voltage at a gate and having a reverse polarity to a polarity of the first correcting transistor, and that generates, in accordance with the second constant voltage, a second correcting current at the second node electrically connected to a drain of the second correcting transistor, wherein

the second node is connected to a connecting node between said second current source and said internal circuit.

24. The semiconductor integrated circuit according to claim 23, wherein:

said bias circuit has a reference voltage generator that has

a threshold voltage compensating function for a variation of a threshold voltage of each of the first transistors formed in said internal circuit and

a temperature compensating function for a temperature variation,

said reference voltage generator generating a constant reference voltage independently of the temperature variation and the variation of the threshold voltage; and

said bias circuit generates the first voltage in accordance with the reference voltage.

25. The semiconductor integrated circuit according to claim 24, wherein

the first constant voltage generator is a band-gap reference.

26. The semiconductor integrated circuit according to claim 23, wherein

one of the first correcting transistor and the second correcting transistor is an nMOS

transistor, and the other is a pMOS transistor.

27. The semiconductor integrated circuit according to claim 23, wherein:

said first current source and said second current source include a second transistor and a third transistor respectively whose gates are connected to the first node; and

the second transistor and the third transistor constitute a first current mirror circuit.

28. The semiconductor integrated circuit according to claim 23, wherein:

a drain of the first correcting transistor is directly connected to the second node;

a drain of the second correcting transistor is connected to each gate of a pair of fourth transistors constituting a second current mirror circuit; and

a drain of one of the fourth transistors not connected to the correcting transistor is connected to the second node.